IN THE CLAIMS:

1. (Currently Amended) A semiconductor device comprising:

a semiconductor substrate;

an MISFET, which is provided on the semiconductor substrate and includes a gate insulating film, a gate electrode and source/drain regions;

a ferroelectric FET, which is provided on the semiconductor substrate and includes a ferroelectric film provided over the semiconductor substrate, a control gate electrode provided on the ferroelectric film and source/drain regions;

a memory circuit block, in which the ferroelectric FET is arranged; ~~and~~

a control circuit block, in which the MISFET is arranged, for controlling the memory circuit block; and

a logic circuit block, in which the MISFET is arranged, including a processor for transferring data to and from the memory circuit block.

2. (Original) The device of claim 1, wherein the ferroelectric FET further includes:

a gate insulating film provided on a part of the substrate, which part is located between the source/drain regions of the ferroelectric FET;

a gate electrode provided on the gate insulating film of the ferroelectric FET;

an interlevel dielectric film covering at least the gate electrode of the ferroelectric FET;

an intermediate electrode provided on the interlevel dielectric film; and

a contact member connecting the intermediate electrode and the gate electrode of the ferroelectric FET together; and

wherein the ferroelectric film is provided on the intermediate electrode.

3. (Original) The device of claim 2, wherein the gate electrode of the ferroelectric FET and the gate electrode of the MISFET are formed out of the same conductor film.

4. (Original) The device of Claim 2, further comprising: a first interconnect connected to the intermediate electrode; and a second interconnect connected to the control gate electrode, and

wherein polarization is created in the ferroelectric film with a voltage applied between the first and the second interconnects.

5. (Cancelled).

6. (Currently Amended) A method for fabricating a semiconductor device, comprising the steps of:

a) forming a gate insulating film and a gate electrode for each of first- and second-channel-type MISFETs and a ferroelectric FET over a semiconductor substrate;

b) implanting ions of a dopant for forming source/drain regions from over the gate electrode of the ferroelectric FET and the gate electrode of one of the first- and second-channel-type MISFETs;

c) implanting ions of another dopant for forming source/drain regions from over the gate electrode of the other MISFET;

d) forming an interlevel dielectric film covering the gate electrodes of the MISFETs and the ferroelectric FET, forming a contact hole, which passes through the interlevel dielectric to reach the gate electrode of the ferroelectric FET, and then filling the contact hole with a conductor material to form a contact member;

e) forming an intermediate electrode, a ferroelectric film and a control gate electrode over the interlevel dielectric film so that the intermediate electrode is connected to the contact member and that the ferroelectric film is in contact with an upper surface of the intermediate electrode and that the control gate electrode faces the intermediate electrode with the ferroelectric film interposed therebetween;

f) forming a memory circuit block, in which the ferroelectric FET is arranged; ~~and~~

g) forming a control circuit block, in which the MISFET is arranged, for controlling the memory circuit block; and

h) forming a logic circuit block, in which the MISFET is arranged, including a processor for transferring data do and from the memory circuit block.

7. (Currently Amended) The method of claim 6, further comprising the steps of:

~~h)~~ i) forming an upper-level dielectric film on the interlevel dielectric film after the step e) has been performed;

~~i)~~ j) forming two contact holes which pass through the upper-level dielectric film to reach the intermediate and control gate electrodes of the ferroelectric FET, respectively, and then filling the contact holes with a conductor material to form first and second contact members, which make electrical contact with the intermediate and control gate electrodes, respectively; and

~~j)~~ k) forming first and second interconnects, which are connected to the first and second contact members, respectively, on the upper-level dielectric film.

REMARKS

The Examiner's non-final Office Action dated November 20, 2003 has been received and its contents carefully noted. Applicants respectfully submit that this response is timely filed and fully responsive to the Office Action.

Claims 1-4, 6 and 7 were pending in the present application, of which claims 1 and 6 are independent. Applicant respectfully contends that no issue of new matter is presented by the aforementioned amendment. Accordingly, claims 1-4, 6 and 7 remain pending, and are believed to be in condition for allowance.

Claims 1-4, 6 and 7 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 4,888,630 to Paterson in view of Japanese Publication No. 11-054717A. In view of the foregoing amendments and comments provided below, Applicants respectfully traverse this rejection.

In accordance with the claimed invention as presently amended, the semiconductor device requires the combination of:

(1) a memory circuit block (in which ferroelectric FETs are arranged), and

(2) a control circuit block (in which MISFETs are arranged) for controlling the memory circuit block,

(3) a logic circuit block (in which MISFETs are arranged), including a processor for transferring data to and from the memory block, with the memory circuit block, the control circuit block and the logic circuit block being provided on the same substrate. As discussed previously, this is advantageous since it allows the formation of a large-scale integrated circuit that is capable of maintaining an increased number of devices.

In contrast, Paterson discloses a memory cell where a ferroelectric FET and a MISFET are formed on the same substrate. Additionally, Japanese Publication No. 11-054717A, is employed in the Office Action, to illustrate the formation of a peripheral control circuit block containing additional MISFETS where the control block is arranged adjacent to the memory circuit block containing the ferroelectric FET.

Applicants respectfully submit that neither Paterson nor Japanese Publication No. 11-054717A teach or suggest a logic circuit block, in which the MISFET is arranged, including a processor for transferring data to and from the memory circuit block, as now recited in independent claim 1, or forming a logic circuit block, in which the MISFET is arranged,

including a processor for transferring data to and from the memory circuit block, as now recited in independent claim 6.

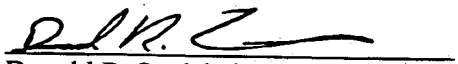
With regard to Paterson, as previously discussed, the path transistor 14 of Paterson is not in the control block of the device. Accordingly, Paterson does not include a logic circuit block, in which the MISFET is arranged, including a processor for transferring data to and from the memory circuit block.

Additionally, Japanese Publication No. 11-054717A discloses that a transistor, or the like, provided in a peripheral circuit area can be formed in a step of fabricating a memory cell (see paragraph [0037] and FIG. 15). However, the peripheral circuit corresponds to the control circuit. Thus, while a peripheral circuit is disclosed outside the area of a memory cell, there is no disclosure of a logic circuit block including a processor for transferring data to and from the memory circuit block, as now recited in independent claims 1 and 6.

Consequently, the teachings of Paterson and Japanese Publication No. 11-054717A do not teach or suggest all features of the presently claimed invention. In particular, Paterson and Japanese Publication No. 11-054717A do not disclose a logic circuit block in which the MISFET is arranged, including a processor for transferring data to and from the memory circuit block, as now recited in independent claim 1, or forming a logic circuit block in which the MISFET is arranged, including a processor for transferring data to and from the memory circuit block, as now recited in independent claim 6. Accordingly, reconsideration and withdrawal of the rejection is earnestly solicited.

Having responded to all rejections set forth in the outstanding non-final Office Action, it is submitted that the claims are now in condition for allowance. An early and favorable Notice of Allowance is respectfully solicited. In the event that the Examiner is of the opinion that a brief telephone or personal interview will facilitate allowance of one or more of the above claims, the Examiner is courteously requested to contact Applicants' undersigned representative.

Respectfully submitted,



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